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Date: 9-19-20

# Submission Instructions:

## Prelab:

1. Complete the prelab (questions Q1 and Q2)
2. Submit this report with the prelab completed to Canvas **before** your lab starts

## Lab:

1. Complete the lab according to the instructions
2. Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.

Complete this report and reupload it to Canvas.

**PRELAB:**

**Q1.** Consider the Verilog code in section 3.0. Briefly explain how the **always @** structure works.

The “always @” block in the code is used to describe an event that are going to happen under certain circumstances. They begin with parenthesis that contain the chosen circumstances; the following block of code must start with a “begin” statement and end with an “end” statement.   
  
**Q2**. Write the Verilog code for ***lab4step1***. Use the example code given in Section 3.0 and make the necessary changes.

module lab4step1 (A, C, G, W, F);

input C, G, W, F;

output A;

reg A;

always @(C or G or W or F)

begin

case ({C,G,W,F})

4'b0000: A= 'b0;

4'b0001: A= 'b0;

4'b0010: A= 'b0;

4'b0011: A= 'b1;

4'b0100: A= 'b0;

4'b0101: A= 'b0;

4’b0110: A=’b1;

4'b0111: A= 'b1;

4'b1000: A= 'b1;

4'b1001: A= 'b1;

4'b1010: A= 'b0;

4'b1011: A= 'b0;

4'b1100: A= 'b1;

4'b1101: A= 'b0;

4'b1110: A= 'b0;

4'b1111: A= 'b0;

endcase

end

endmodule

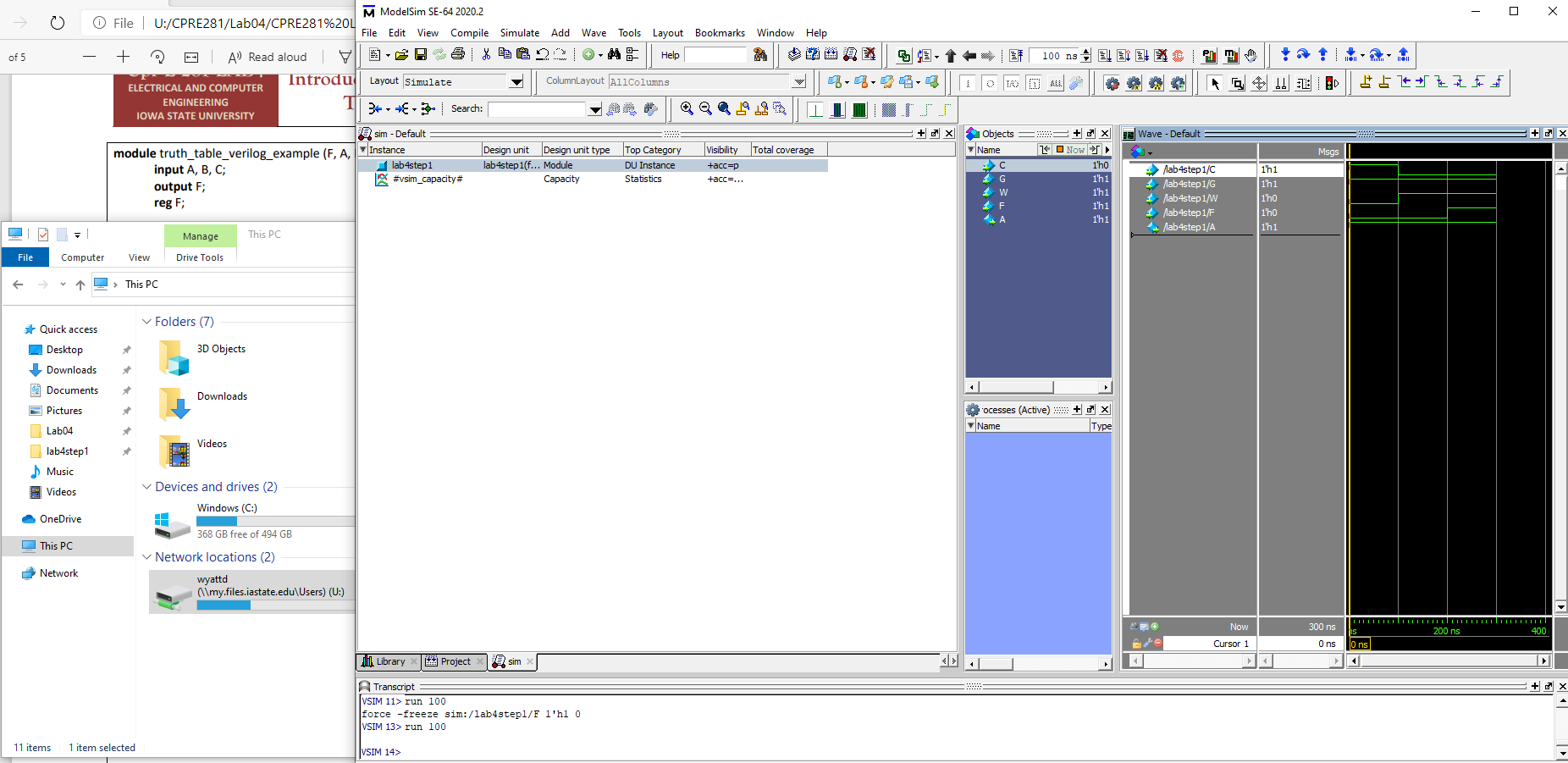
**Q3**. Read Section 4.0 and fill in the Truth Table for ***lab4step2***.

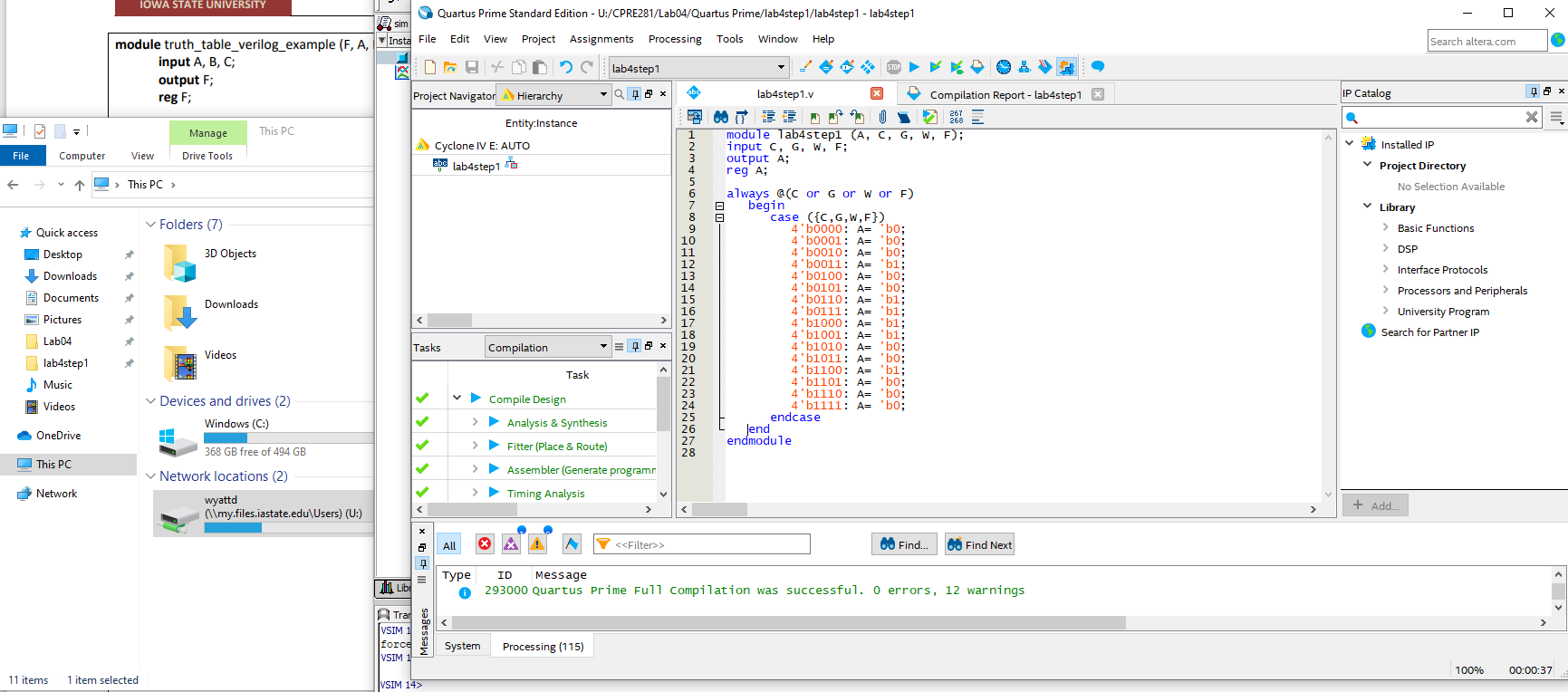
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | **Outputs** | | |
| **M** | **T** | **H** | **P** | **E** | **F** | **AC** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**LAB:  
3.0** Use the hardware results to fill in the truth table for ***lab4step1.***

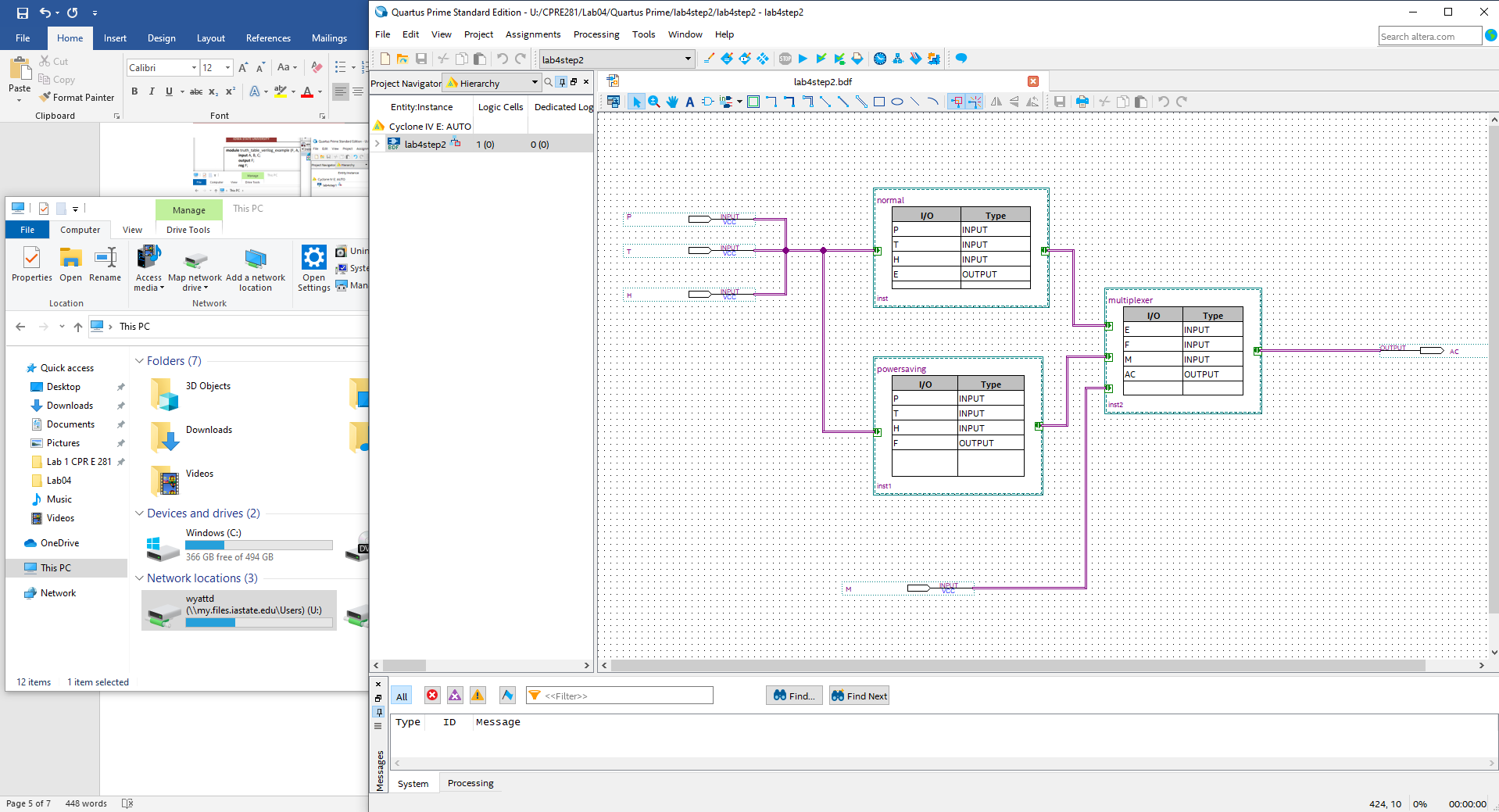
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Farmer** | **Cabbage** | **Goat** | **Wolf** | **Alarm** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 |

Screenshots:



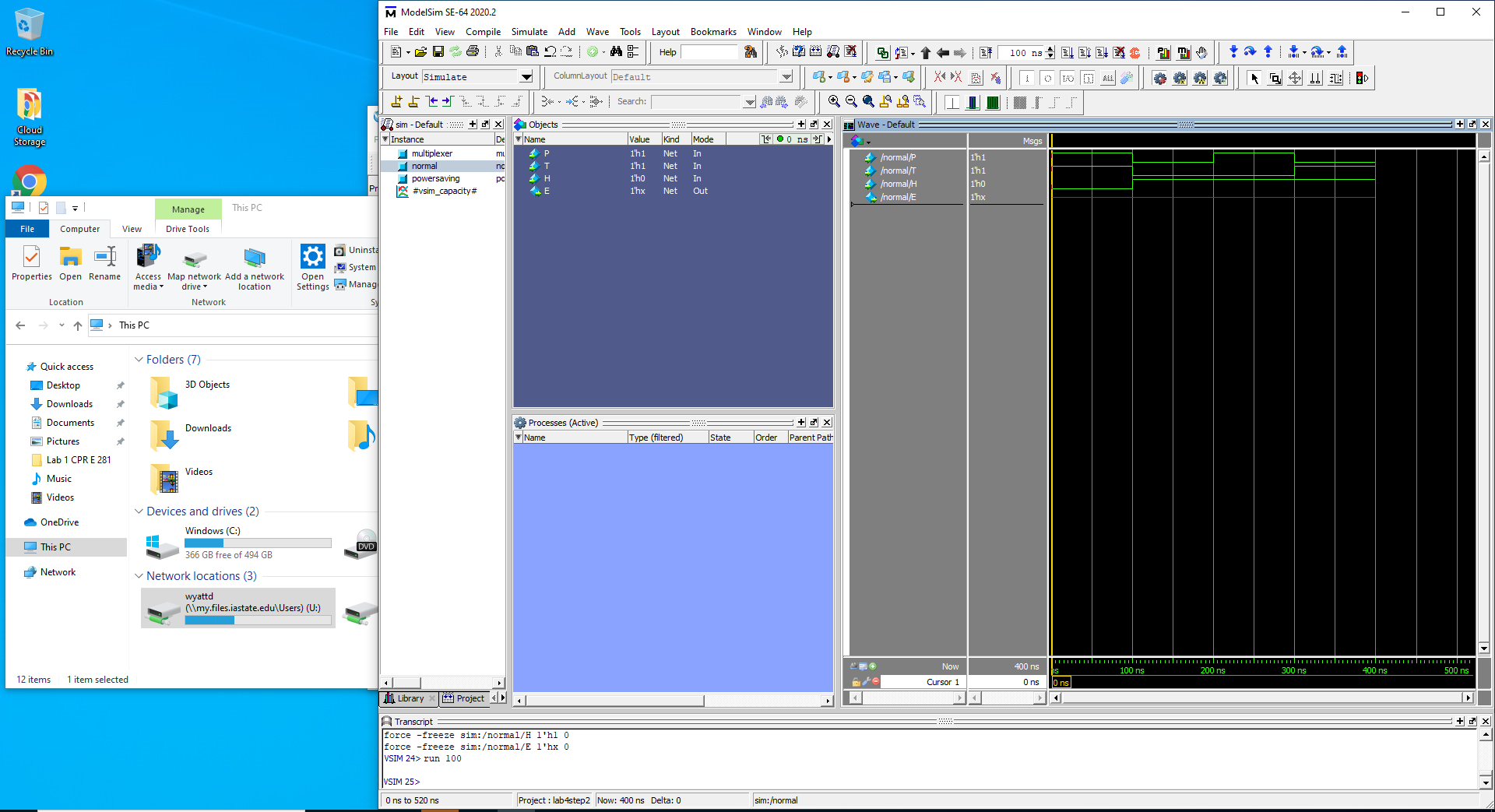


**4.0**  Demonstrate hardware results for correct code.

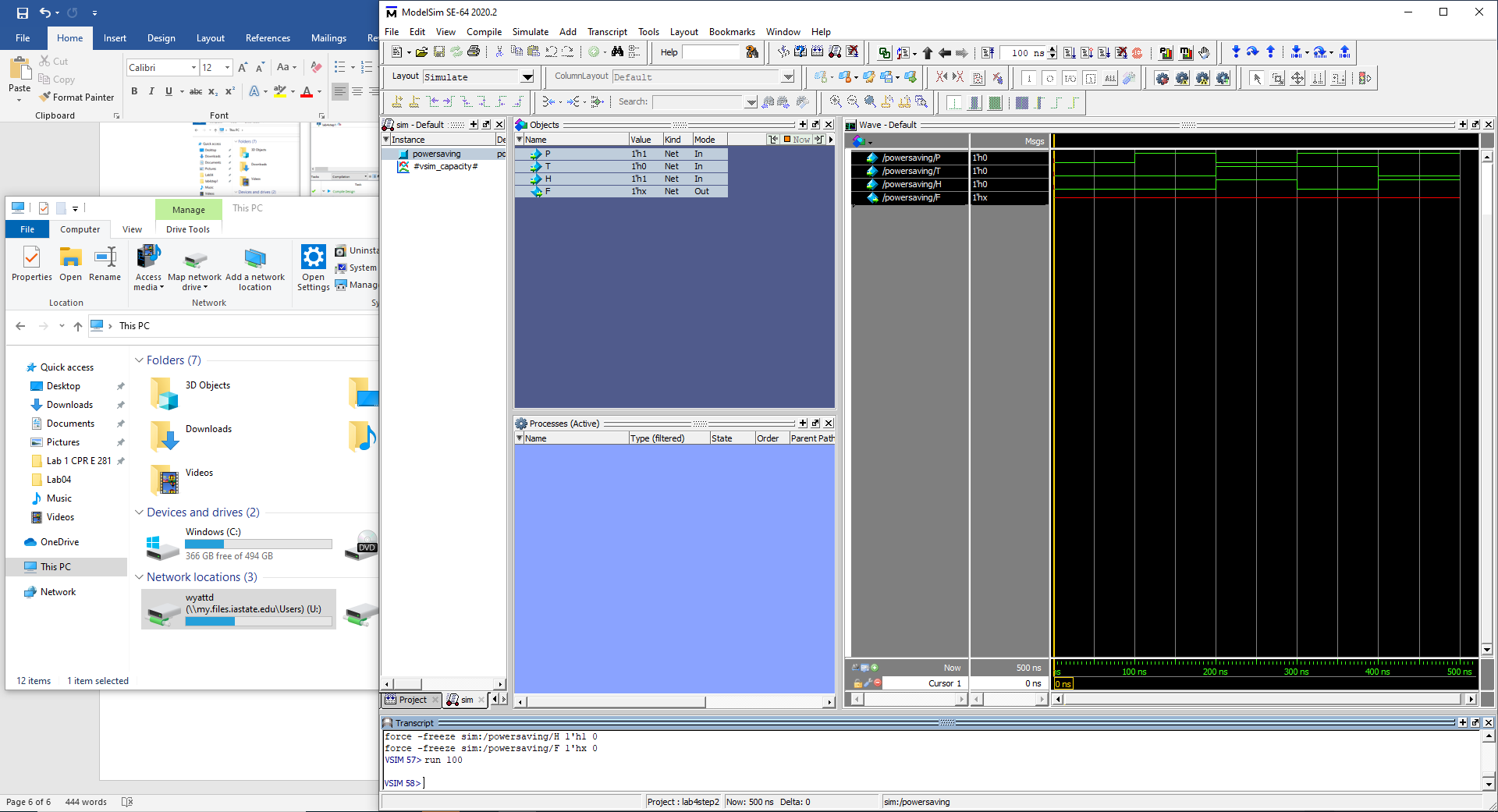


**Design result:**

Normal:



Power Saving:



Multiplexer:

